Amendments to the Claims

1. (CURRENTLY AMENDED) An active matrix display device comprising an array ~~(34)~~ of pixels arranged in rows and columns, wherein each column of pixels shares a column conductor ~~(12)~~ to which pixel drive signals are provided, wherein column address circuitry ~~(32)~~ is provided for generating the pixel drive signals, the column address circuitry comprising an output buffer ~~(46)~~ for providing a pixel drive signal to a column conductor, wherein the positive and negative slew rates of the output buffer are different.

2. (CURRENTLY AMENDED) A device as claimed in claim 1, wherein the output buffer comprises a first transistor ~~(54)~~ connected between the column conductor ~~(12)~~ and a high power line and a second transistor ~~(56)~~ connected between the column conductor and a low power line, wherein the slew rates of the first and second transistors are different.

3. (CURRENTLY AMENDED) A device as claimed in claim 2, wherein the first transistor ~~(54)~~ comprises a p-type transistor and the second transistor ~~(56)~~ comprises an n-type transistor, and wherein the first and second transistors are switched simultaneously.

4. (CURRENLTY AMENDED) A device as claimed in ~~any preceding claim,~~claim 1 wherein the pixels are driven in different frames with different polarity pixel drive signals, and wherein the pixel charging time from a first drive signal, having a first polarity and corresponding to a given brightness, to a second drive signal, having the opposite polarity and corresponding to the same given brightness, is substantially equal to the pixel charging time from the second drive signal to the first drive signal.

5. (CURRENTLY AMENDED) A device as claimed in ~~any preceding claim,~~claim 1 wherein each pixel comprises an n-type switching transistor ~~(14),~~ and wherein the negative slew rate is lower than the positive slew rate.

6. (CURRENTLY AMENDED) A device as claimed in claim 5, wherein the output buffer comprises a first transistor ~~(54)~~ connected between the column conductor and a high power line and a second transistor ~~(56)~~ connected between the column conductor and a low power line, wherein the second transistor has a lower maximum current drive than the first

transistor.

7. (CURRENLTY AMENDED) A device as claimed in ~~anyone of claims 1 to 4,~~claim 1 wherein each pixel comprises a p-type switching transistor, and wherein the positive slew rate is lower than the negative slew rate.

8. (CURRENTLY AMENDED) A device as claimed in claim 7, wherein the output buffer comprises a first transistor ~~(54)~~ connected between the column conductor and a high power line and a second transistor ~~(56)~~ connected between the column conductor and a low power line, wherein the first transistor has a lower maximum current drive than the second transistor.

9. (CURRENTLY AMENDED) A device as claimed in ~~any preceding claim,~~ claim 1 comprising an output buffer ~~(46)~~ for each column.

10. (CURRENTLY AMENDED) A device as claimed in ~~any preceding claim,~~claim 1 comprising an active matrix LCD display device.

11. (ORIGINAL) Column address circuitry for driving the columns of an active matrix display, comprising an output buffer for providing a pixel drive signal to a column conductor, wherein the positive and negative slew rates of the output buffer are different.